High Speed, Low Noise Video Op Amp

AD829

FEATURES

High Speed
- **120 MHz Bandwidth, Gain = –1**
- **230 V/μs Slew Rate**
- **90 ns Settling Time to 0.1%**

Ideal for Video Applications
- **0.02% Differential Gain**
- **0.04° Differential Phase**

Low Noise
- **1.7 nV/√Hz Input Voltage Noise**
- **1.5 pA/√Hz Input Current Noise**

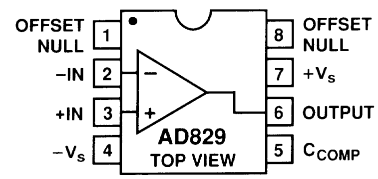
Excellent DC Precision
- **1 mV max Input Offset Voltage (Over Temp)**
- **0.3 μV/°C Input Offset Drift**

Flexible Operation
- **Specified for ±5 V to ±15 V Operation**
- **±3 V Output Swing into a 150 Ω Load**
- **External Compensation for Gains 1 to 20**
- **5 mA Supply Current**

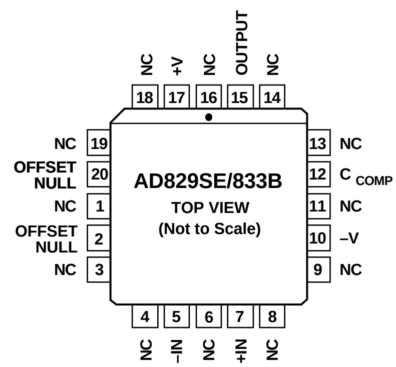
Available in Tape and Reel in Accordance with EIA-481A Standard

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



20-Pin LCC Pinout



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD829 is a low noise (1.7 nV/√Hz), high speed op amp with custom compensation that provides the user with gains from ±1 to ±20 while maintaining a bandwidth greater than 50 MHz. The AD829's 0.04° differential phase and 0.02% differential gain performance at 3.58 MHz and 4.43 MHz, driving reverse-terminated 50 Ω or 75 Ω cables, makes it ideally suited for professional video applications. The AD829 achieves its 230 V/μs uncompensated slew rate and 750 MHz gain bandwidth product while requiring only 5 mA of current from the power supplies.

The AD829's external compensation pin gives it exceptional versatility. For example, compensation can be selected to optimize the bandwidth for a given load and power supply voltage. As a gain-of-two line driver, the –3 dB bandwidth can be increased to 95 MHz at the expense of 1 dB of peaking. In addition, the AD829's output can also be clamped at its external compensation pin.

The AD829 has excellent dc performance. It offers a minimum open-loop gain of 30 V/mV into loads as low as 500 Ω, low input voltage noise of 1.7 nV/√Hz, and a low input offset voltage of 1 mV maximum. Common-mode rejection and power supply rejection ratios are both 120 dB.

The AD829 is also useful in multichannel, high speed data conversion where its fast (90 ns to 0.1%) settling time is of importance. In such applications, the AD829 serves as an input buffer for 8-to-10-bit A/D converters and as an output I/V converter for high speed D/A converters.

The AD829 provides many of the same advantages that a transimpedance amplifier offers, while operating as a traditional voltage feedback amplifier. A bandwidth greater than 50 MHz can be maintained for a range of gains by changing the external compensation capacitor. The AD829 and the transimpedance amplifier are both unity gain stable and provide similar voltage noise performance (1.7 nV/√Hz). However, the current noise of the AD829 (1.5 pA/√Hz) is less than 10% of the noise of transimpedance amps. Furthermore, the inputs of the AD829 are symmetrical.

PRODUCT HIGHLIGHTS

1. Input voltage noise of 2 nV/√Hz, current noise of 1.5 pA/√Hz and 50 MHz bandwidth, for gains of 1 to 20, make the AD829 an ideal preamp.
2. Differential phase error of 0.04° and a 0.02% differential gain error, at the 3.58 MHz NTSC and 4.43 MHz PAL and SECAM color subcarrier frequencies, make it an outstanding video performer for driving reverse-terminated 50 Ω and 75 Ω cables to ±1 V (at their terminated end).
3. The AD829 can drive heavy capacitive loads.
4. Performance is fully specified for operation from ±5 V to ±15 V supplies.
5. Available in plastic, cerdip, and small outline packages. Chips and MIL-STD-883B parts are also available.

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD829—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.2	1		0.1	0.5	mV
	T_{MIN} to T_{MAX}				1			0.5	mV
Offset Voltage Drift		±5 V, ±15 V		0.3			0.3		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	7		3.3	7	µA
	T_{MIN} to T_{MAX}				8.2			9.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	500		50	500	nA
	T_{MIN} to T_{MAX}				500			500	nA
Offset Current Drift		±5 V, ±15 V		0.5			0.5		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		30	65		30	65		V/mV
	T_{MIN} to T_{MAX}		20			20			V/mV
	R_{LOAD} = 150 Ω			40			40		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		50	100		50	100		V/mV
	T_{MIN} to T_{MAX}		20			20			V/mV
	R_{LOAD} = 500 Ω			85			85		V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth Product		±5 V		600			600		MHz
		±15 V		750			750		MHz
Full Power Bandwidth[1, 2]	V_O = 2 V p-p								
	R_{LOAD} = 500 Ω	±5 V		25			25		MHz
	V_O = 20 V p-p								
	R_{LOAD} = 1 kΩ	±15 V		3.6			3.6		MHz
Slew Rate[2]	R_{LOAD} = 500 Ω	±5 V		150			150		V/µs
	R_{LOAD} = 1 kΩ	±15 V		230			230		V/µs
Settling Time to 0.1%	A_V = –19								
	–2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step	±15 V		90			90		ns
Phase Margin[2]	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			60			60		Degrees
DIFFERENTIAL GAIN ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.02			0.02		%
DIFFERENTIAL PHASE ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.04			0.04		Degrees
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	100	120		100	120		dB
	V_{CM} = ±12 V	±15 V	100	120		100	120		dB
	T_{MIN} to T_{MAX}		96			96			dB
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V		98	120		98	120		dB
	T_{MIN} to T_{MAX}		94			94			dB
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		1.7	2		1.7	2	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				–3.8			–3.8		V
		±15 V		+14.3			+14.3		V
				–13.8			–13.8		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} 50 Ω	±5 V		1.4			1.4		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short Circuit Current		±5 V, ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance (Differential)				13			13		kΩ
Input Capacitance (Differential)[4]				5			5		pF
Input Capacitance (Common Mode)				1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			2			2		mΩ

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		5	6.5		5	6.5	mA
	T_{MIN} to T_{MAX}				8.0			8.2/8.7	mA
		±15 V		5.3	6.8		5.3	6.8	mA
	T_{MIN} to T_{MAX}				8.3			8.5/9.0	mA
TRANSISTOR COUNT	Number of Transistors			46			46		

NOTES
[1]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[2]Tested at Gain = +20, C_{COMP} = 0 pF.
[3]3.58 MHz (NTSC) and 4.43 MHz (PAL & SECAM).
[4]Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.
Specifications subject to change without notice.

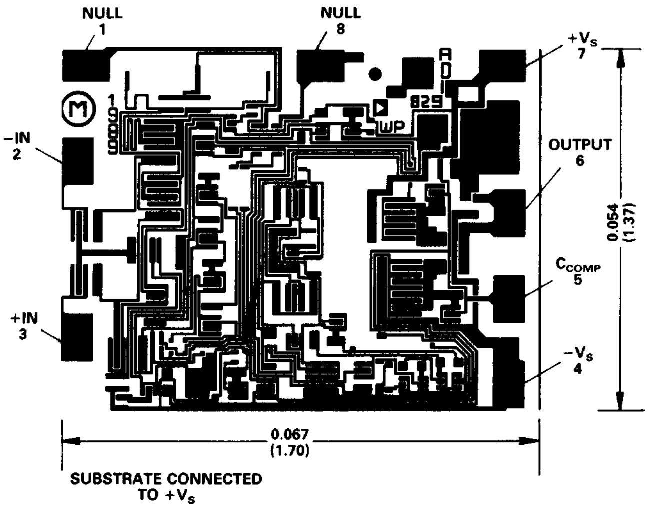
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipations[2]
  Plastic (N) . . . . 1.3 Watts
  Small Outline (R) . . . . 0.9 Watts
  Cerdip (Q) . . . . 1.3 Watts
  LCC (E) . . . . 0.8 Watts
Input Voltage . . . . $\pm V_S$
Differential Input Voltage[3] . . . . ±6 Volts
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range (Q, E) . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range
  AD829J . . . . 0°C to +70°C
  AD829A . . . . –40°C to +85°C
  AD829S . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.
Thermal characteristics:
8-pin plastic package: θ_{JA} = 100°C/watt (derate at 8.7 mW/°C)
8-pin cerdip package: θ_{JA} = 110°C/watt (derate at 8.7 mW/°C)
20-pin LCC package: θ_{JA} = 150°C/watt
8-pin small outline package: θ_{JA} = 155°C/watt (derate at 6 mW/°C).
[3]If the differential voltage exceeds 6 volts, external series protection resistors should be added to limit the input current.

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD829 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD829JN	0°C to +70°C	8-Pin Plastic Mini-DIP	N-8
AD829JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD829JR-REEL	0°C to +70°C	Tape & Reel	
AD829AQ	–40°C to +85°C	8-Pin Cerdip	Q-8
AD829SQ	–55°C to +125°C	8-Pin Cerdip	Q-8
AD829SQ/883B	–55°C to +125°C	8-Pin Cerdip	Q-8
5962-9312901MPA	–55°C to +125°C	8-Pin Cerdip	Q-8
AD829SE/883B	–55°C to +125°C	20-Pin LCC	E-20A
5962-9312901M2A	–55°C to +125°C	20-Pin LCC	E-20A
AD829JChips	0°C to +70°C	Die	
AD829SChips	–55°C to +125°C	Die	

*E = Leadless Chip Carrier (Ceramic); N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC).

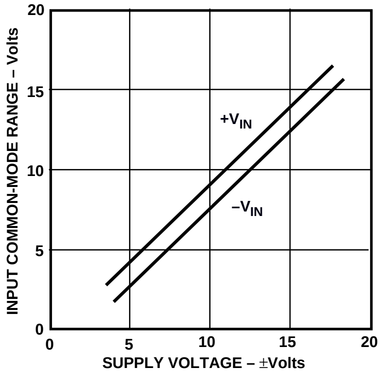


Figure 1. Input Common-Mode Range vs. Supply Voltage

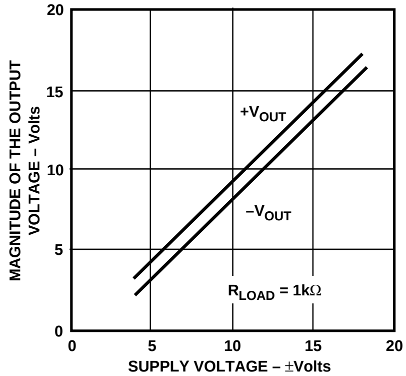


Figure 2. Output Voltage Swing vs. Supply Voltage

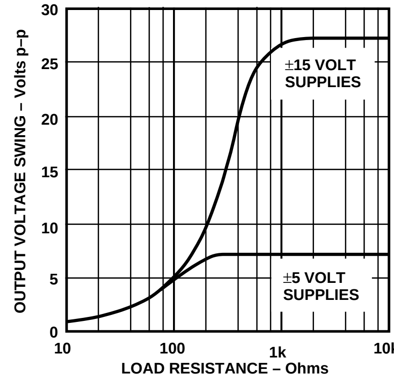


Figure 3. Output Voltage Swing vs. Resistive Load

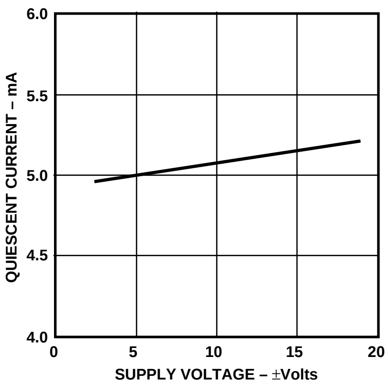


Figure 4. Quiescent Current vs. Supply Voltage

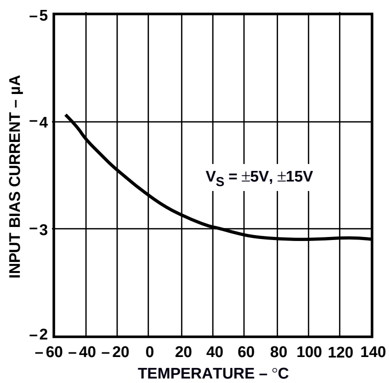


Figure 5. Input Bias Current vs. Temperature

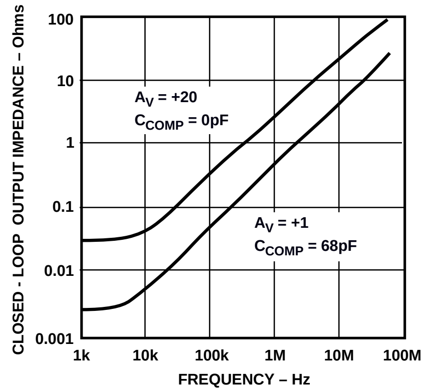


Figure 6. Closed-Loop Output Impedance vs. Frequency

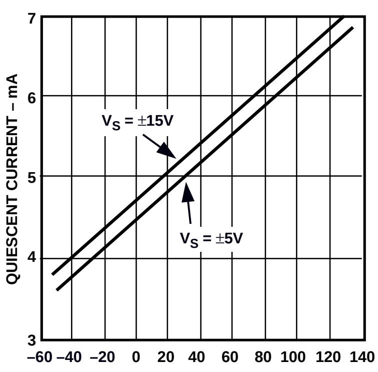


Figure 7. Quiescent Current vs. Temperature

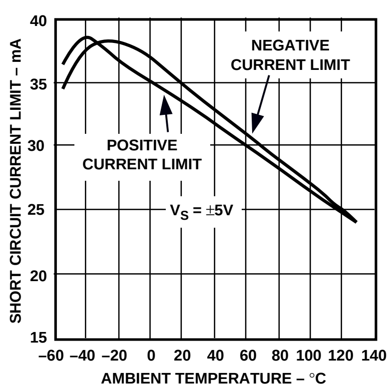


Figure 8. Short Circuit Current Limit vs. Temperature

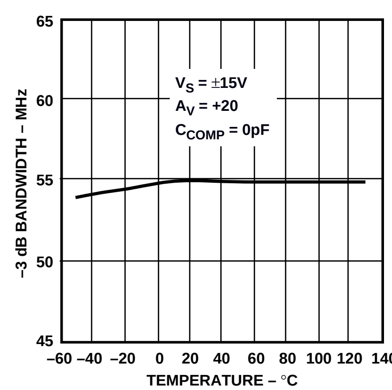


Figure 9. –3 dB Bandwidth vs. Temperature

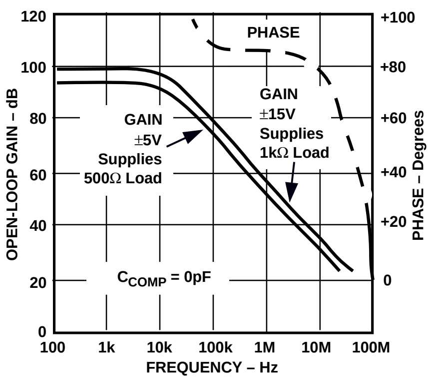


Figure 10. Open-Loop Gain & Phase Margin vs. Frequency

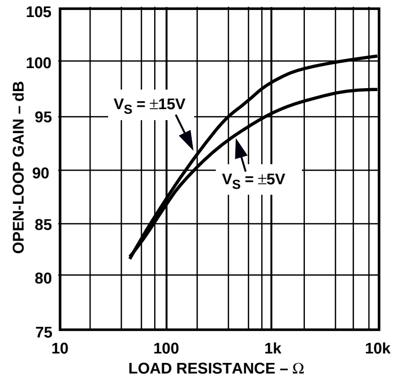


Figure 11. Open-Loop Gain vs. Resistive Load

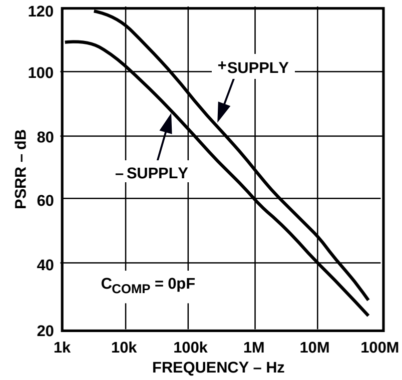


Figure 12. Power Supply Rejection Ratio (PSRR) vs. Frequency

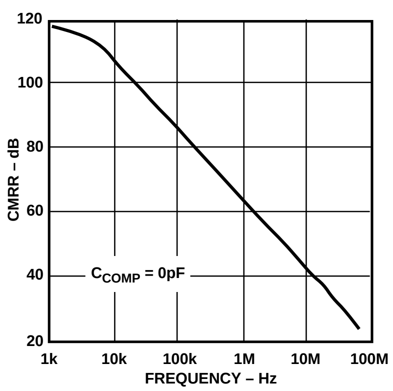


Figure 13. Common-Mode Rejection Ratio vs. Frequency

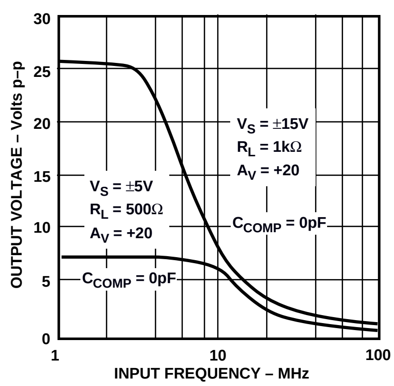


Figure 14. Large Signal Frequency Response

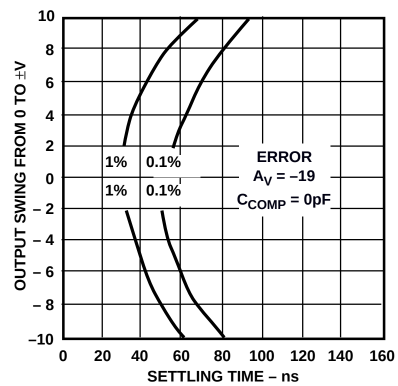


Figure 15. Output Swing & Error vs. Settling Time

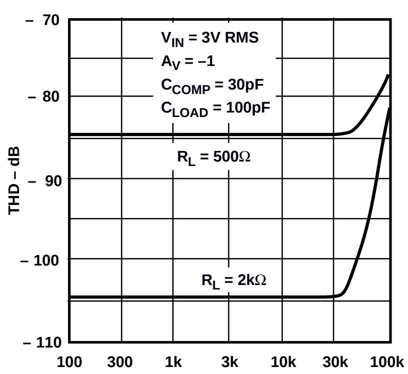


Figure 16. Total Harmonic Distortion (THD) vs. Frequency

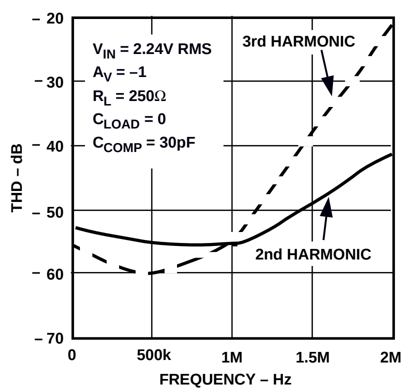


Figure 17. 2nd & 3rd Harmonic Distortion vs. Frequency

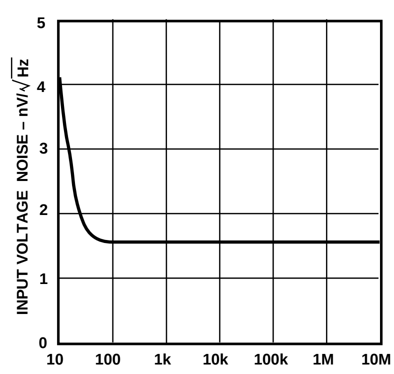


Figure 18. Input Voltage Noise Spectral Density

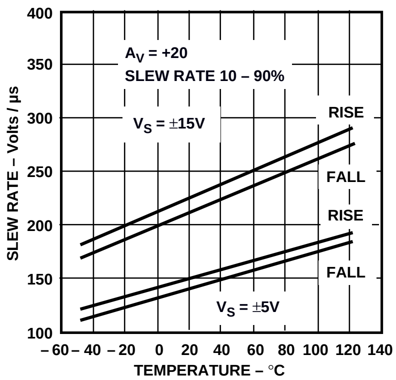


Figure 19. Slew Rate vs. Temperature

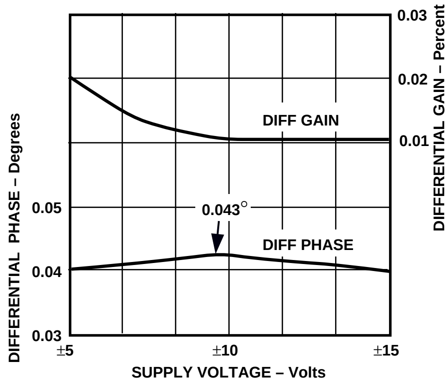


Figure 20. Differential Gain & Phase vs. Supply

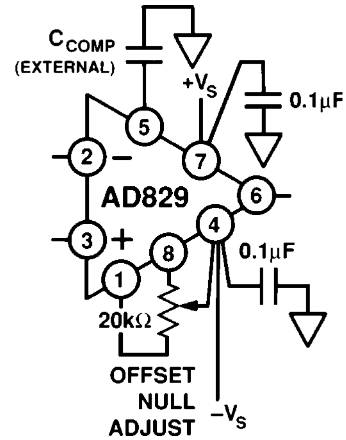


Figure 21. Offset Null and External Shunt Compensation Connections

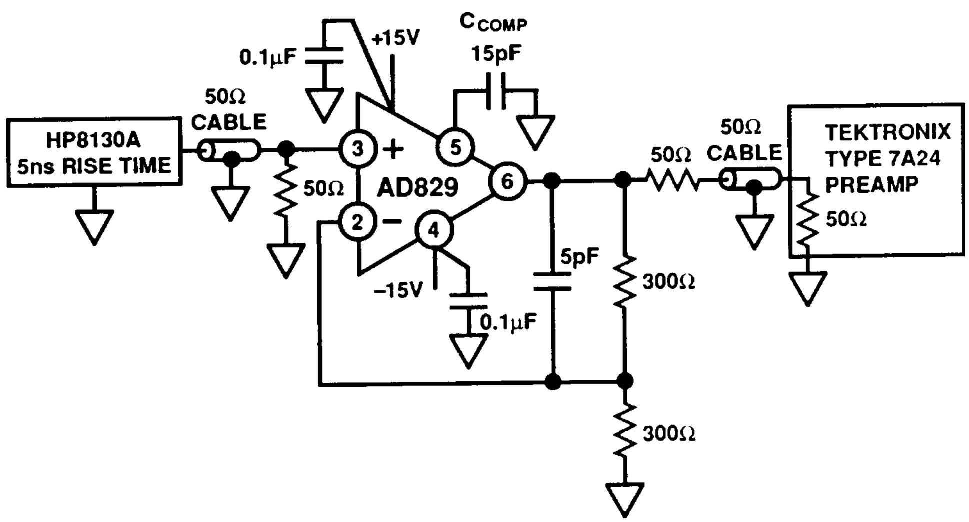


Figure 22a. Follower Connection. Gain = +2

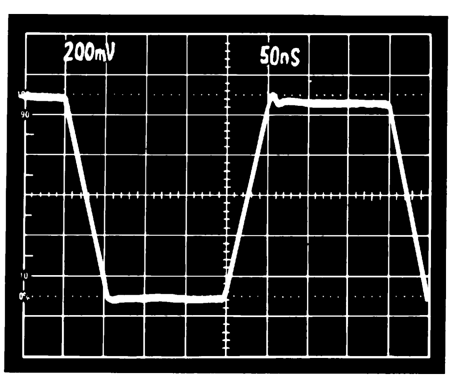


Figure 22b. Gain of 2 Follower Large Signal Pulse Response

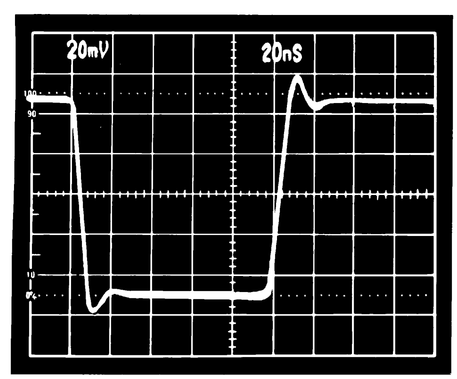


Figure 22c. Gain of 2 Follower Small Signal Pulse Response

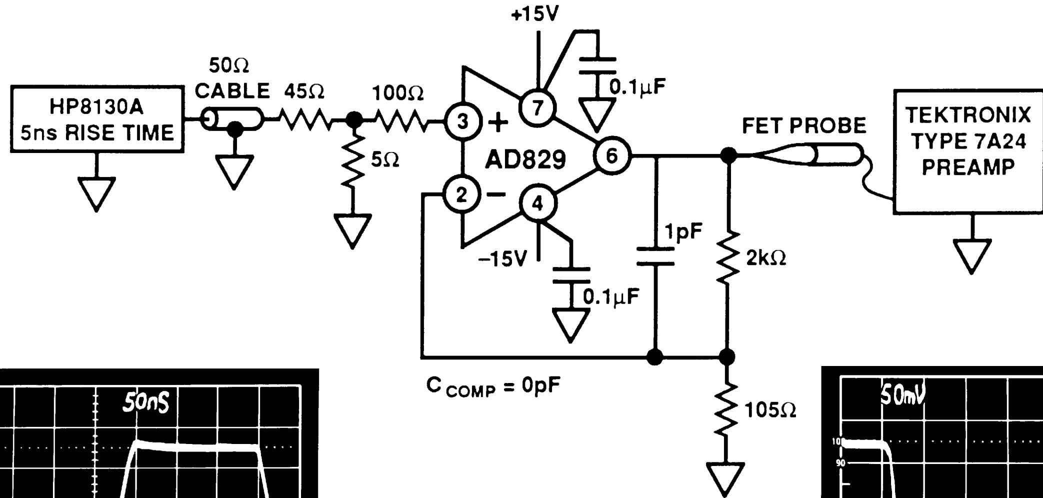


Figure 23a. Follower Connection. Gain= + 20

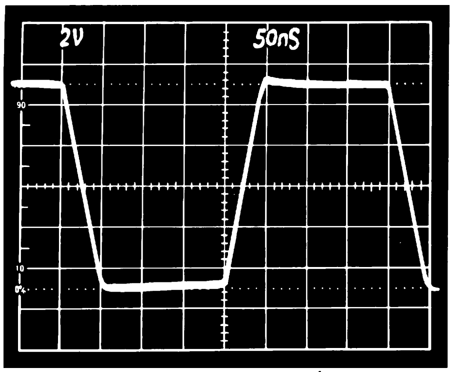


Figure 23b. Gain of 20 Follower Large Signal Pulse Response

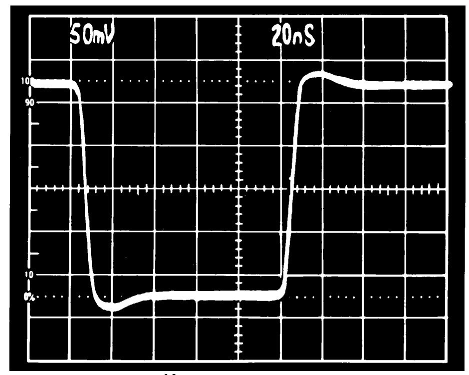


Figure 23c. Gain of 20 Follower Small Signal Pulse Response

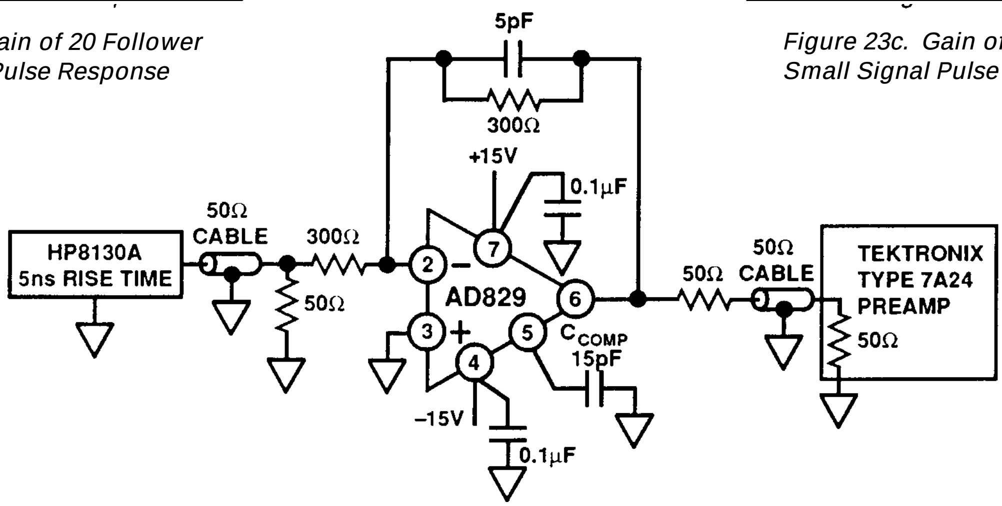


Figure 24a. Unity Gain Inverter Connection

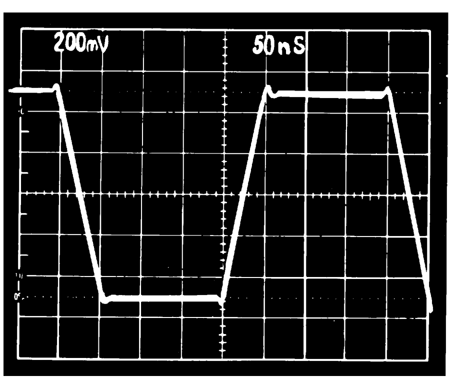


Figure 24b. Unity Gain Inverter Large Signal Pulse Response

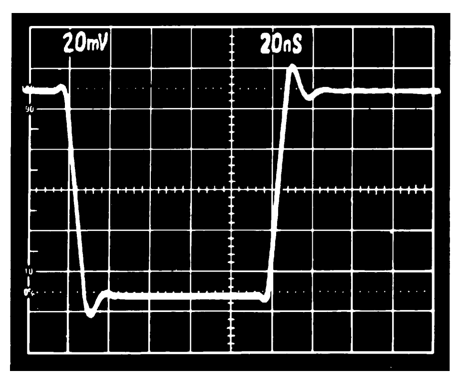


Figure 24c. Unity Gain Inverter Small Signal Pulse Response

THEORY OF OPERATION

The AD829 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process which provides PNP and NPN transistors with similar f_Ts of 600 MHz. As shown in Figure 25, the AD829 input stage consists of an NPN differential pair in which each transistor operates at 600 μA collector current. This gives the input devices a high transconductance and hence gives the AD829 a low noise figure of 2 nV/$\sqrt{Hz}$ @ 1 kHz.

The input stage drives a folded cascode which consists of a fast pair of PNP transistors. These PNPs then drive a current mirror which provides a differential-input to single-ended-output conversion. The high speed PNPs are also used in the current-amplifying output stage which provides high current gain of 40,000. Even under conditions of heavy loading, the high f_Ts of the NPN & PNPs, produced using the CB process, permit cascading two stages of emitter followers while still maintaining 60° of phase margin at closed-loop bandwidths greater than 50 MHz.

Two stages of complementary emitter followers also effectively buffer the high impedance compensation node (at the C_{COMP} pin) from the output so that the AD829 can maintain a high dc open-loop gain, even into low load impedances: 92 dB into a 150 Ω load, 100 dB into a 1 kΩ load. Laser trimming and PTAT biasing assure low offset voltage and low offset voltage drift enabling the user to eliminate ac coupling in many applications.

For added flexibility, the AD829 provides access to the internal frequency compensation node. This allows the user to customize frequency response characteristics for a particular application.

Unity gain stability requires a compensation capacitance of 68 pF (Pin 5 to ground) which will yield a small signal bandwidth of 66 MHz and slew rate of 16 V/μs. The slew rate and gain bandwidth product will vary inversely with compensation capacitance. Table I and the graph of Figure 28 show the optimum compensation capacitance and the resulting slew rate for a desired noise gain. For gains between 1 and 20, C_{COMP} can be chosen to keep the small signal bandwidth relatively constant. The minimum gain which will still provide stability also depends on the value of external compensation capacitance.

An RC network in the output stage (Figure 25) completely removes the effect of capacitive loading when the amplifier is compensated for closed-loop gains of 10 or higher. At low frequencies, and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C is bootstrapped and does not contribute to the compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage– this reduces the gain, and subsequently, C is incompletely bootstrapped. Therefore, some fraction of C contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is further increased, the bandwidth continues to fall, and the amplifier remains stable.

Externally Compensating the AD829

The AD829 is stable with no external compensation for noise gains greater than 20. For lower gains, there are two methods of frequency compensating the amplifier to achieve closed-loop stability; these are the shunt and current feedback compensation methods.

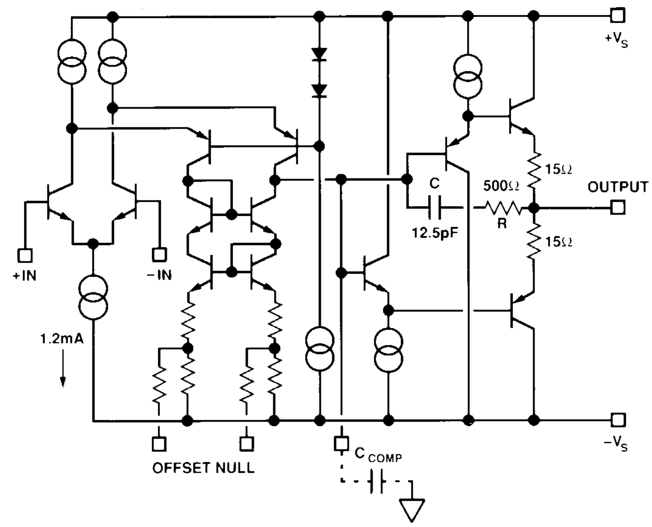


Figure 25. AD829 Simplified Schematic

Shunt Compensation

Figures 26 & 27 show that the first method, shunt compensation, has an external compensation capacitor, C_{COMP}, connected between the compensation pin and ground. This external capacitor is tied in parallel with approximately 3 pF of internal capacitance at the compensation node. In addition, a small capacitance, C_{LEAD}, in parallel with resistor R2, compensates for the capacitance at the amplifier's inverting input.

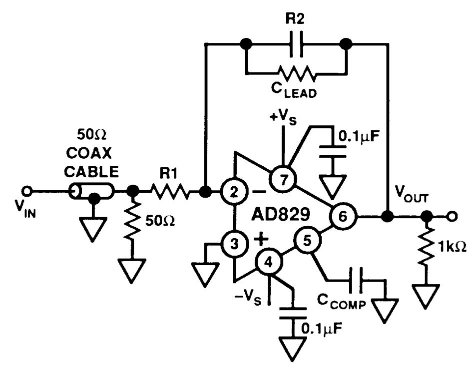


Figure 26. Inverting Amplifier Connection Using External Shunt Compensation

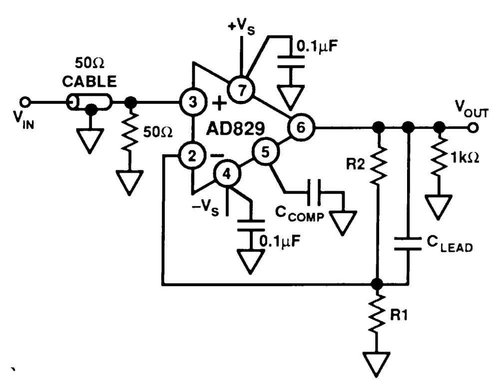


Figure 27. Noninverting Amplifier Connection Using External Shunt Compensation

Table I. Component Selection for Shunt Compensation

Follower Gain	Inverter Gain	R1 Ω	R2 Ω	C_L pF	C_{COMP} pF	Slew Rate V/µs	–3 dB Small Signal Bandwidth – MHz
1		Open	100	0	68	16	66
2	–1	1k	1k	5	25	38	71
5	–4	511	2.k	1	7	90	76
10	–9	226	2.5k	0	3	130	65
20	–19	105	2k	0	0	230	55
25	–24	105	2.49	0	0	230	39
100	–99	20	2k	0	0	230	7.5

Table I gives recommended C_{COMP} and C_{LEAD} values along with the corresponding slew rates and bandwidth. The capacitor values given were selected to provide a small signal frequency response with less than 1 dB of peaking and less than 10% overshoot. For this table, supply voltages of ±15 volts should be used. Figure 28 is a graphical extension of the table which shows the slew rate/gain trade-off for lower closed-loop gains, when using the shunt compensation scheme.

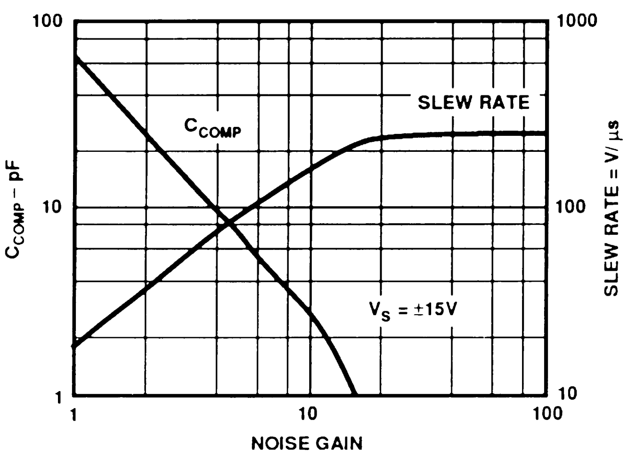


Figure 28. Value of C_{COMP} & Slew Rate vs. Noise Gain

Current Feedback Compensation

Bipolar nondegenerated amplifiers which are single pole and internally compensated have their bandwidths defined as:

$$f_T = \frac{1}{2\pi r_e C_{COMP}} = \frac{I}{2\pi \frac{kT}{q} C_{COMP}}$$

where:

f_T is the unity gain bandwidth of the amplifier
I is the collector current of the input transistor
C_{COMP} is the compensation capacitance
r_e is the inverse of the transconductance of the input transistors
kT/q is approximately equal to 26 mV @ 27°C.

Since both f_T and slew rate are functions of the same variables, the dynamic behavior of an amplifier is limited. Since:

$$Slew\ Rate = \frac{2I}{C_{COMP}}$$

then:

$$\frac{Slew\ Rate}{f_T} = 4\pi \frac{kT}{q}$$

This shows that the slew rate will be only 0.314 V/µs for every MHz of bandwidth. The only way to increase slew rate is to increase the f_T and that is difficult, due to process limitations. Unfortunately, an amplifier with a bandwidth of 10 MHz can only slew at 3.1 V/µs, which is barely enough to provide a full power bandwidth of 50 kHz.

The AD829 is especially suited to a new form of compensation which allows for the enhancement of both the full power bandwidth and slew rate of the amplifier. The voltage gain from the inverting input pin to the compensation pin is large; therefore, if a capacitance is inserted between these pins, the amplifier's bandwidth becomes a function of its feedback resistor and this capacitance. The slew rate of the amplifier is now a function of its internal bias (2I) and this compensation capacitance.

Since the closed-loop bandwidth is a function of R_F and C_{COMP} (Figure 29), it is independent of the amplifier closed-loop gain, as shown in Figure 31. To preserve stability, the time constant of R_F and C_{COMP} needs to provide a bandwidth of less than 65 MHz. For example, with C_{COMP} = 15 pF and R_F = 1 kΩ, the small signal bandwidth of the AD829 is 10 MHz, while Figure 30 shows that the slew rate is in excess of 60 V/µs. As can be seen in Figure 31, the closed-loop bandwidth is constant for gains of –1 to –4, a property of current feedback amplifiers.

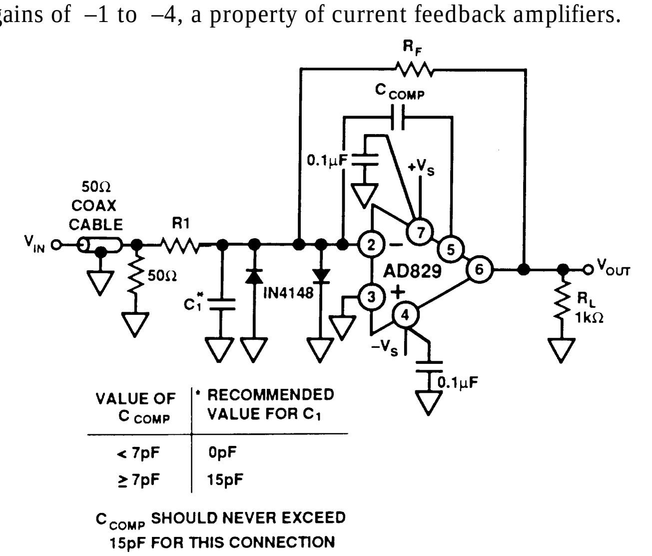


Figure 29. Inverting Amplifier Connection Using Current Feedback Compensation

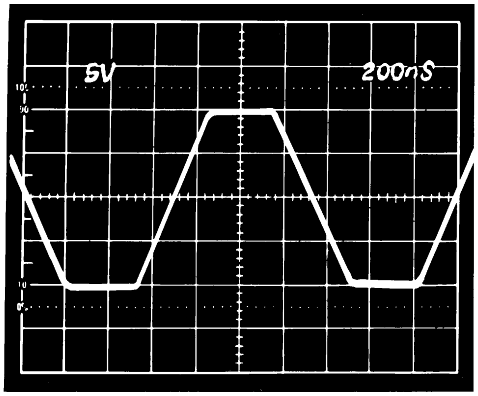


Figure 30. Large Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation. C_{COMP} = 15 pF, C1 = 15 pF, R_F = 1 kΩ, R1 = 1 kΩ

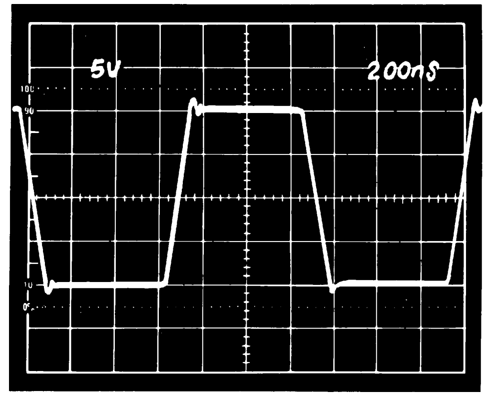


Figure 32. Large Signal Pulse Response of the Inverting Amplifier Using Current Feedback Compensation. C_{COMP} = 1 pF, R_F = 3 kΩ, R1 = 3 kΩ

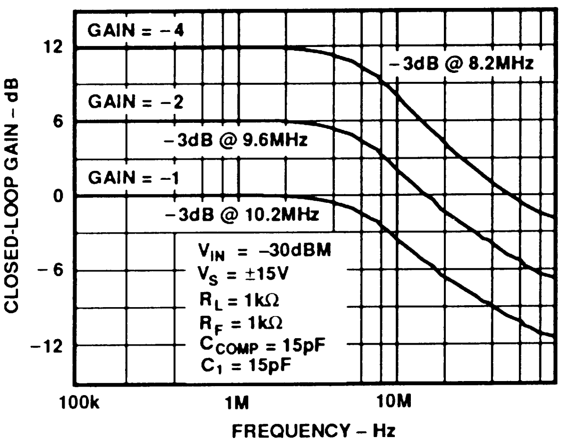


Figure 31. Closed-Loop Gain vs. Frequency for the Circuit of Figure 29

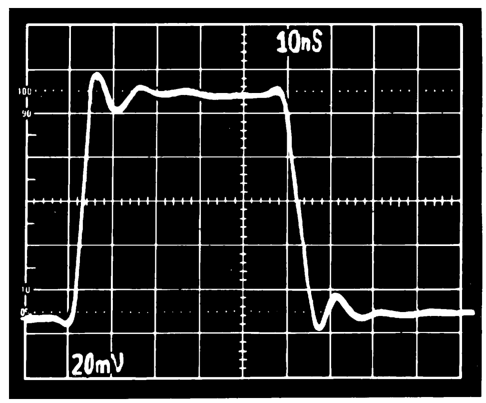


Figure 33. Small Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation. C_{COMP} = 4 pF, R_F = 1 kΩ, R1 = 1 kΩ

Figure 32 is an oscilloscope photo of the pulse response of a unity gain inverter which has been configured to provide a small signal bandwidth of 53 MHz and a subsequent slew rate of 180 V/µs; resistor R_F = 3 kΩ, capacitor C_{COMP} = 1 pF. Figure 33 shows the excellent pulse response as a unity gain inverter, this time using component values of: R_F = 1 kΩ and C_{COMP} = 4 pF.

Figures 34 and 35 show the closed-loop frequency response of the AD829 for different closed-loop gains and for different supply voltages.

If a noninverting amplifier configuration using current feedback compensation is desired, the circuit of Figure 36 is recommended. This circuit doubles the slew rate compared to the shunt compensated noninverting amplifier of Figure 27 at the expense of gain flatness. Nonetheless, this circuit delivers 95 MHz bandwidth with ±1 dB flatness into a back terminated cable, with a differential gain error of only 0.01%, and a differential phase error of only 0.015° at 4.43 MHz.

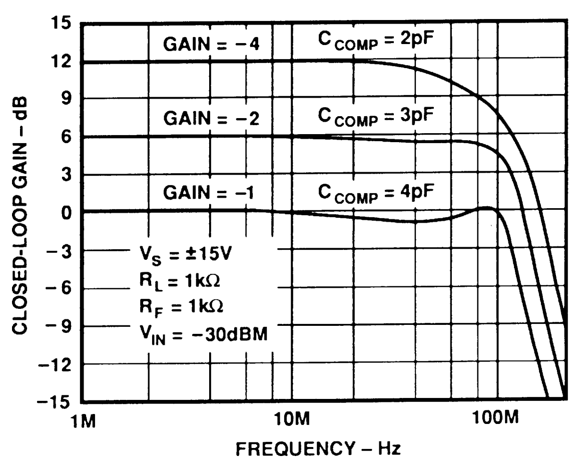


Figure 34. Closed-Loop Frequency Response for the Inverting Amplifier Using Current Feedback Compensation

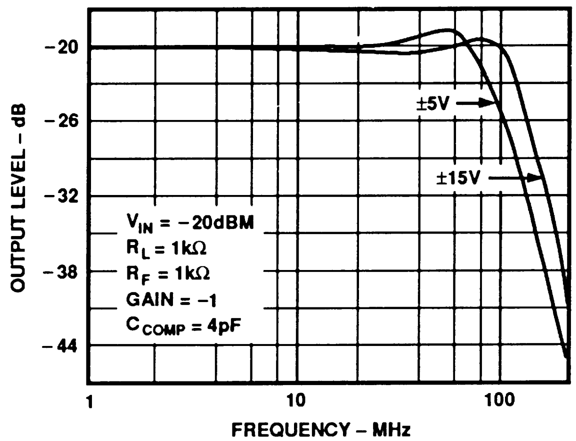


Figure 35. Closed-Loop Frequency Response vs. Supply for the Inverting Amplifier Using Current Feedback Compensation

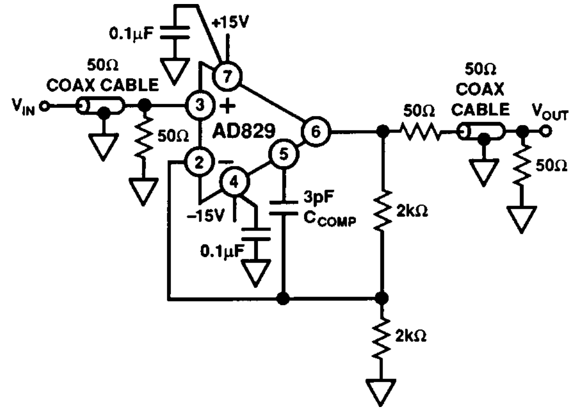


Figure 36. Noninverting Amplifier Connection Using Current Feedback Compensation

A Low Error Video Line Driver

The buffer circuit shown in Figure 37 will drive a back-terminated 75 Ω video line to standard video levels (1 V p-p) with 0.1 dB gain flatness to 30 MHz with only 0.04° and 0.02% differential phase and gain at the 4.43 MHz PAL color subcarrier frequency. This level of performance, which meets the requirements for high definition video displays and test equipment, is achieved using only 5 mA quiescent current.

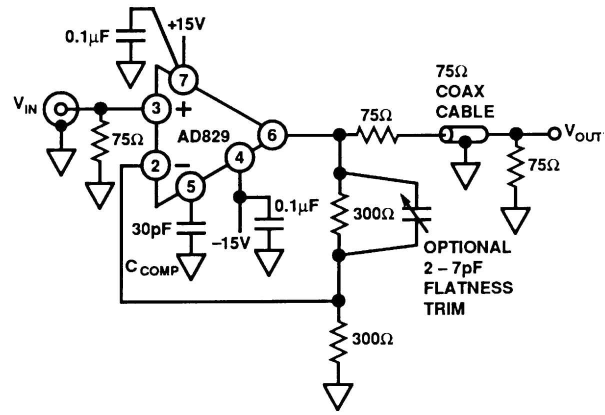
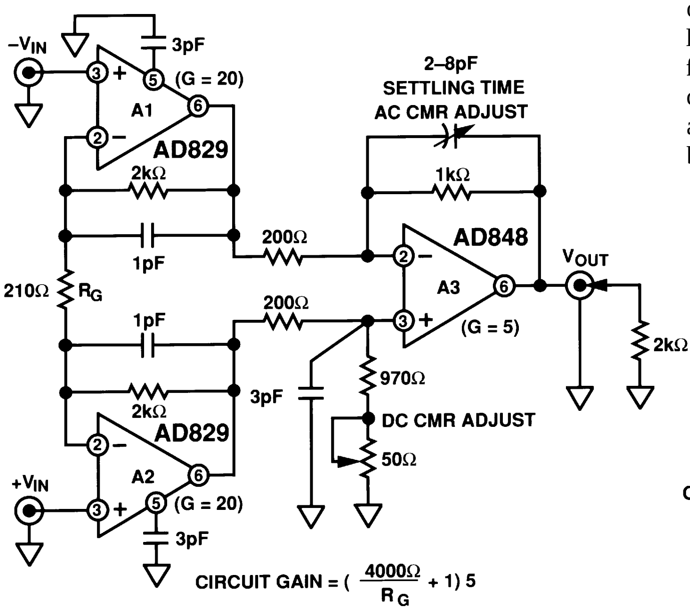


Figure 37. A Video Line Driver with a Flatness over Frequency Adjustment

A High Gain, Video Bandwidth Three Op Amp In Amp

Figure 38 shows a three op amp instrumentation amplifier circuit which provides a gain of 100 at video bandwidths. At a circuit gain of 100 the small signal bandwidth equals 18 MHz into an FET probe. Small signal bandwidth equals 6.6 MHz with a 50 Ω load. 0.1% settling time is 300 ns.

The input amplifiers operate at a gain of 20, while the output op amp runs at a gain of 5. In this circuit the main bandwidth limitation is the gain/ bandwidth product of the output amplifier. Extra care needs to be taken while breadboarding this circuit, since even a couple of extra picofarads of stray capacitance at the compensation pins of A1 and A2 will degrade circuit bandwidth.



INPUT FREQUENCY	CMRR
100 Hz	64.6 dB
1 MHz	44.7 dB
10 MHz	23.9 dB

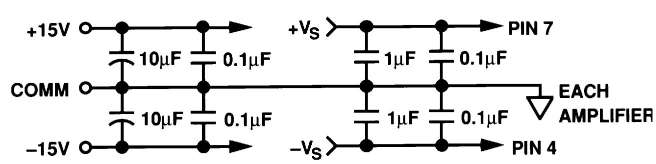
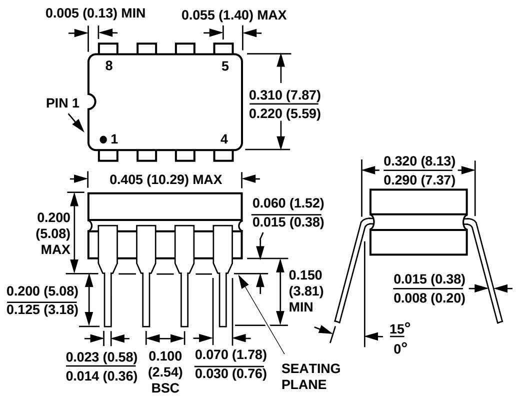


Figure 38. A High Gain, Video Bandwidth Three Op Amp In Amp Circuit

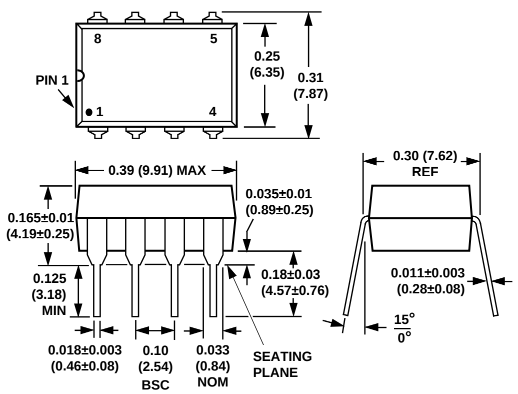
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

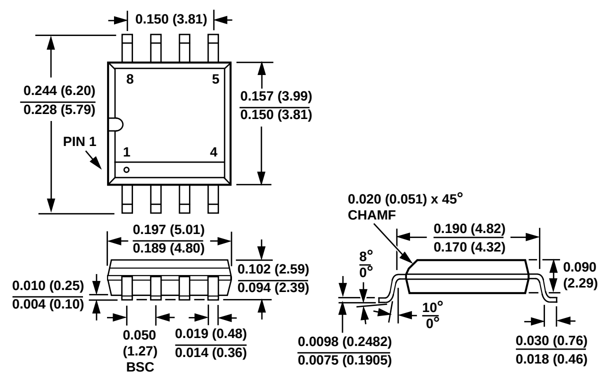
Cerdip (Q) Package



Plastic Mini-DIP (N) Package



8-Pin SOIC (R) Package



C1443b–10–10/92

PRINTED IN U.S.A.